Customer No.: 31561
Application No.: 10/710,933
Docket No.: 11537-US-PA

REMARKS

Present Status of Application

The Office Action dated December 16, 2005, objected drawings for not shown every feature of the claims. Claims 1-4, 6 and 7 were rejected under 35 USC§102(e) as being anticipated by Terui (US Patent No. 6,534,879). Claims 1, 3, 5 and 16-18 were rejected under 35 USC§102(b) as being anticipated by Giri et al. (US Patent No. 6,261,467).

Claim 1 has been amended for providing more descriptions for clarification purposes, while claim 4 has been cancelled. No new matter has been added to the application by the amendments made to the specification, claims and drawings. This Amendment is promptly filed to place the above-captioned case in condition for allowance. After entering the amendments and considering the following discussions, a notice of allowance is respectfully solicited.

Discussion for the objections of drawings

The Office Action dated December 16, 2005, objected drawings for not shown every feature of the claims. Especially, "the chip is electrically connected to the chip carrier through wire bonding technology" as recited in claim 4.

Claim 4 has been cancelled.

Withdrawn of this objection is respectfully requested.

Discussion for 35 USC§102 rejections

Claims 1-4, 6 and 7 were rejected under 35 USC§102(e) as being anticipated by Terui (US Patent No. 6,534,879). Claims 1, 3, 5 and 16-18 were rejected under 35 USC§102(b) as being anticipated by Giri et al. (US Patent No. 6,261,467).

Claim 1 has been amended for clarification purposes.

Applicants submit that independent claim 1 or 16 patently defines over the prior references for at least the reason that the cited art fails to disclose each and every feature as claimed in the present invention.

As amended, the independent claim 1 recites:

*1. **A quad flat no-lead package structure**, comprising:*
a chip carrier having a top surface and a bottom surface, wherein a plurality of conductive leads is disposed on the bottom surface of the chip carrier, while a plurality of pads is disposed on the top surface of the chip carrier, the conductive leads being electrically connected to the pads; and
*at least a chip, disposed on the top surface of the chip carrier and electrically connected to the chip carrier, **wherein the chip covers at least a portion of the pads on the top surface of the chip carrier.***

The Office Action considered that the reference Terui substantially discloses all the features of this invention as recited in claims 1-4 and 6-7. The Office Action considered Terui's substrate 10, pad & solder balls 30/40 and chip 60 comparable to the chip carrier, the conductive leads and the chip of this invention.

Applicants respectfully traverse this interpretation.

Terui discloses a semiconductor chip having a plurality of electrodes on its main surface and, more specifically, to such a semiconductor chip being suitable for a ball grid array (BGA) type semiconductor device (see Field of the Invention). Further, the structure as taught in Terui's Figure 3A-3B is directed a semiconductor device 100 including a substrate 10, pads 30 and ball electrodes 40 (made of solder) on the pads 30 (col. 4, lines 1-6). Chip 60 is mounted on the substrate 10. As taught by Terui, solder ball electrodes 40 are connected to the printed board (col. 13, lines 35-39). Clearly, Terui teaches a BGA type semiconductor device with solder balls for further connection with the printed board.

In this case, even considering chip 60 is comparable to the chip of this invention, Terui does not teaches the conductive leads of this invention because Terui in fact teaches solder balls, rather than conductive leads. Moreover, Terui teaches the BGA type package structure having a plurality of solder balls on the bottom surface of the substrate, whereas the present invention is directed to a quad flat no-lead (QFN) package structure having a plurality of conductive leads on the bottom surface of the chip carrier. As known to one of ordinary skilled in the art, the technology applied to a QFN package structure is vastly different for the technology applied to a BGA type package structure.

Accordingly, the QFN package structure of the present invention is patentably

distinct from the prior art reference Terui because Terui fails to disclose all limitations of claim 1. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Applicant respectfully asserts that the structure of the amended claim 1 or 16 is patentably distinct from the structure of the reference Giri.

Giri discloses **a ceramic carrier** 100 including joining pads 118 on the top surface 114 and pads/pins 121/122 on the bottom surface 116. Giri teaches "Pads in the conductor layer 120 on the ceramic carrier's bottom surface 116 may be braze pads 121 for attaching pins 122 for pin grid array (PGA) attachment. Alternatively, the pads may be direct mount pads 121' for directly attaching the module 100 onto a printed circuit board. Also, the pads may be solder attach pads 121", used in, for example, what is commonly referred to in the art as land grid array (LGA), ball grid array (BGA), column grid array (CGA) or miniBGA." (see col. 3, lines 1-9). Obviously, Giri's ceramic module is not a QFN package structure and Giri's pads/pins 121/122 will not be considered as comparable to the conductive leads of this invention, to one of ordinary skills in the art.

Moreover, Giri also fails to disclose a wafer-level package structure comprising a wafer and a plurality of conductive blocks in each of the sections of the wafer. Clearly, Giri's top surface 114 of the ceramic substrate 100 can not be construed as comparable to

a wafer, as indicated by the Office Action Further, since Giri's joining pads 118 are formed on the top or bottom surface 114/116, the pads 118 should not be considered as bonding pads of the chip as recited in claim 16. Applicants therefore respectfully traverse the interpretations of the Office Action based on the reference Giri.

Accordingly, the structure of the present invention is patentably distinct from the prior art reference Giri because Giri fails to disclose all limitations of claim 1 or 16. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Consequently, reconsideration and withdrawal of these 102 rejections are respectfully requested.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw